IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of: **Yasuo ONISHI, et al.** Group Art Unit: **2629**

Serial Number: **09/774,099** Examiner: **Alecia Diane Nelson**

Filed: **January 31, 2001** Confirmation Number: **1075**

For: **DISPLAY DEVICE AND PIXEL CORRESPONDING DISPLAY DEVICE**

Attorney Docket Number: **010093**
Customer Number: **38834**

SUBMISSION OF APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

August 24, 2006

Sir:

Applicants submit herewith an Appeal Brief in the above-identified U.S. patent application.

Attached please find a check in the amount of $500.00 to cover the cost for the Appeal Brief. If any additional fees are due in connection with this submission, please charge Deposit Account No. 50-2866.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

APPEAL BRIEF FOR THE APPELLANT

Ex parte Yasuo ONISHI et al. (Applicant)

DISPLAY DEVICE AND PIXEL CORRESPONDING DISPLAY DEVICE

Serial Number: 09/774,099

Filed: January 31, 2001

Appeal No.:

Group Art Unit: 2629

Examiner: Alecia Diane Nelson

Submitted by:
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August 24, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of: **Yasuo ONISHI, et al.**

Appeal No.: Unassigned
Group Art Unit: **2629**
Examiner: **Alecia Diane Nelson**

Serial Number: **09/774,099**

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Attorney Docket Number: **010093**
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APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 24, 2006

Sir:

Applicants appeal the January 26, 2006 rejection of claims 1-6.

Following the Notice of Appeal filed on June 26, 2006, the following is the Applicants' (now referred to hereinbelow as "appellants") Appeal Brief.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the subject application, which is:

Sanyo Electric Co., Ltd, 5-5, Keihanhondori 2-chome, Morguchi City, Osaka 570-8677, Japan by an assignment recorded in the U.S. Patent and Trademark Office on July 10, 2001, at Reel 011962, Frame 0089.

II. RELATED APPEALS AND INTERFERENCES

Appellants know of no other appeals or interference proceedings related to the present appeal.

III. STATUS OF CLAIMS

Claims 1-6 stand rejected. Claims 7 and 8 are allowed. The claims on appeal are claims 1-6.

IV. STATUS OF AMENDMENTS

An Amendment was filed under 37 CFR 1.111 on March 30, 2004 in which claims 1, 3, 5 and 6 were amended. An Amendment was filed under 37 CFR 1.111 on April 29, 2005 in which claims 1 and 3 were amended. Each of these Amendments has been entered.

The list of claims in the Claim Appendix includes the claims as last amended in the Amendment filed April 29, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to a display device and pixel corresponding display.

With respect to claim 1, a display device comprising: a clock generation circuit (see, *e.g.*, sampling clock adjustment circuit 40 in Fig. 2 and 3; and page 25, lines 10-20) for generating sampling clocks, whose frequency is controlled on the basis of a required frequency control value, on the basis of a horizontal synchronizing signal of an input video signal;

an analog-to-digital converter (see, *e.g.*, A/D converters 2R, 2G, 2B in Fig. 2; and page 25, lines 2-5) for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

horizontal video start position detection means (see, *e.g.*, horizontal video start/end detection circuit 61 in Fig. 3; and page 28, lines 12-19) for detecting a horizontal video start position of video data outputted from the analog-to-digital converter on the basis of a first threshold value;

horizontal video end position detection means (see, e.g., horizontal video start/end detection circuit 61 in Fig. 3; page 29, lines 12-19; and page 30, lines 4-8) for detecting a horizontal video end position of the video data outputted from the analog-to-digital converter on the basis of a variable second threshold value;

calculation means (see, *e.g.*, H counter 62 in Fig. 3; and page 30, line 11 – page 31, line 7) for calculating the number of sampling clocks corresponding to the distance from the horizontal video start position to the horizontal video end position;

judgment means (see, *e.g.*, maximum hold unit 63, subtracter 64 and comparator 65 in Fig. 3; and page 31, line 16 - page 32, line 24) for judging whether or not the result of the calculation by the calculation means coincides with a required reference value;

frequency control value adjustment means (see, *e.g.*, CPU 66 in Fig. 3; and page 32, line 25 – page 34, line 1) for calculating, when it is judged that the result of the calculation by the calculation means and the reference value do not coincide with each other, a new frequency control value on the basis of the result of the calculation by the calculation means, the reference

value, and the frequency control value currently set in the clock generation circuit, to feed the new frequency control value to the clock generation circuit; and

threshold value control means (see, *e.g.*, threshold value control unit 67 in Fig. 3; and page 41, line 17 – page 43, line 20) for controlling, for each vertical period, the variable second threshold value depending on the level of the video data at the horizontal video end position detected within the vertical period.

With respect to claim 3, a display device comprising: a clock generation circuit (see, *e.g.*, sampling clock adjustment circuit 40 in Fig. 2 and 3; and page 25, lines 10-20) for generating sampling clocks, whose frequency is controlled on the basis of a required frequency control value, on the basis of a horizontal synchronizing signal of an input video signal;

an analog-to-digital converter (see, *e.g.*, A/D converters 2R, 2G, 2B in Fig. 2; and page 25, lines 2-5) for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

a horizontal video start position detection circuit (see, *e.g.*, horizontal video start/end detection circuit 61 in Fig. 3; and page 28, lines 12-19) for detecting a horizontal video start position of video data outputted from the analog-to-digital converter on the basis of a first threshold value;

a horizontal video end position detection circuit (see, e.g., horizontal video start/end detection circuit 61 in Fig. 3; page 29, lines 12-19; and page 30, lines 4-8) for detecting a horizontal video end position of the video data outputted from the analog-to-digital converter on the basis of a variable second threshold value;

a calculation circuit (see, *e.g.*, H counter 62 in Fig. 3; and page 30, line 11 – page 31, line 7) for calculating the number of sampling clocks corresponding to the distance from the horizontal video start position to the horizontal video end position;

a judgment circuit (see, *e.g.*, maximum hold unit 63, subtracter 64 and comparator 65 in Fig. 3; and page 31, line 16 - page 32, line 24) for judging whether or not the result of the calculation by the calculation means coincides with a required reference value;

a frequency control value adjustment circuit (see, *e.g.*, CPU 66 in Fig. 3; and page 32, line 25 – page 34, line 1) for calculating, when it is judged that the result of the calculation by the calculation circuit and the reference value do not coincide with each other, a new frequency control value on the basis of the result of the calculation by the calculation circuit, the reference value, and the frequency control value currently set in the clock generation circuit, to feed the new frequency control value to the clock generation circuit; and

a threshold value control means (see, *e.g.*, threshold value control unit 67 in Fig. 3; and page 41, line 17 – page 43, line 20) for controlling, for each vertical period, the variable second threshold value depending on the level of the video data at the horizontal video end position detected within the vertical period.

With respect to claim 5, a pixel corresponding display device comprising a clock generation circuit (see, *e.g.*, clock generation circuit 92 in Fig. 7; and page 45, lines 11-23) for generating sampling clocks on the basis of a horizontal synchronizing signal of an input video signal;

an analog-to-digital converter (see, *e.g.*, A/D converters 2R, 2G, 2B in Fig. 7; and page 45, lines 11-23) for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

detection means (see, *e.g.*, horizontal video start/end detection circuit 81 in Fig. 7; and page 46, lines 1 - 26) for comparing video data outputted from the analog-to-digital converter with a predetermined threshold value, to detect a horizontal video start position and a horizontal video end position on each of horizontal lines;

calculation means (see, *e.g.*, H counter 82, maximum hold unit 83, subtracter 84, absolute value circuit 85 and field integration averaging circuit 86 in Fig. 7; and page 47, line 20 – page 49, line 3) for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal out of horizontal video start positions detected within one field and a horizontal video end position farthest from the horizontal period start position specified by the horizontal synchronizing signal out of horizontal video end positions detected within one field, the number of sampling clocks corresponding to the distance between the horizontal video start position and the horizontal video end position of the input video signal for the field;

frequency adjustment means (see, *e.g.*, clock frequency detection circuit 88 and cpu 90 in Fig, 7; and page 49, lines 4 – page 50, line 1) for controlling the clock generation circuit on the basis of the result of the calculation by the calculation means, to adjust the frequency of the sampling clocks;

judgment means (see, *e.g.*, display region narrow video detection circuit 87 in Fig. 7; and page 51, lines 9 – 24) for judging for each field whether or not the width of a region where input

video exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation means; and

means for stopping (see, *e.g.*, cpu 90 in Fig. 7; page 52, lines 1-8; and page 53, line 24 – page 54, line 13), while the width of the region where the input video exists is being judged to be smaller than the number of horizontal effective pixels, a frequency adjustment operation based on the number of sampling clocks found in the field.

With respect to claim 6, a pixel corresponding display device comprising:

a clock generation circuit (see, *e.g.*, clock generation circuit 92 in Fig. 7; and page 45, lines 11-23) for generating sampling clocks on the basis of a horizontal synchronizing signal of an input video signal;

an analog-to-digital converter (see, *e.g.*, A/D converters 2R, 2G, 2B in Fig. 7; and page 45, lines 11-23) for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

a detection circuit (see, *e.g.*, horizontal video start/end detection circuit 81 in Fig. 7; and page 46, lines 1 - 26) for comparing video data outputted from the analog-to-digital converter with a predetermined threshold value, to detect a horizontal video start position and a horizontal video end position on each of horizontal lines;

a calculation circuit (see, *e.g.*, H counter 82, maximum hold unit 83, subtracter 84, absolute value circuit 85 and field integration averaging circuit 86 in Fig. 7; and page 47, line 20 – page 49, line 3) for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal out of horizontal

video start positions detected within one field and a horizontal video end position farthest from a horizontal period start position specified by the horizontal synchronizing signal out of horizontal video end positions detected within one field, the number of sampling clocks corresponding to the distance between the horizontal video start position and the horizontal video end position of the input video signal for the field;

a frequency adjustment circuit (see, *e.g.*, clock frequency detection circuit 88 and cpu 90 in Fig, 7; and page 49, lines 4 – page 50, line 1) for controlling the clock generation circuit on the basis of the result of the calculation by the calculation circuit, to adjust the frequency of the sampling clocks;

a judgment circuit (see, *e.g.*, display region narrow video detection circuit 87 in Fig. 7; and page 51, lines 9 – 24) for judging for each field whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation circuit; and

a circuit for stopping (see, *e.g.*, cpu 90 in Fig. 7; page 52, lines 1-8; and page 53, line 24 – page 54, line 13), while the width of the region where the input video exists is being judged to be smaller than the number of horizontal effective pixels, a frequency adjustment operation based on the number of sampling clocks found in the field.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The rejection of claims 1-6 under 35 U.S.C. § 103(a) as being unpatentable over Koike (EP 0 953 963).

VII. ARGUMENTS

A. Rejection of claims 1-6 under 35 U.S.C. § 103(a) as being unpatentable over Koike

Claims 1 -4

Independent claim 1 calls for a *horizontal video end position detection means for detecting a horizontal video end position of the video data outputted from the analog-to-digital converter on the basis of a variable second threshold value; ... threshold value control means for controlling, for each vertical period, the variable second threshold value depending on the level of the video data at the horizontal video end position detected within the vertical period.* Independent claim 3 includes similar features.

It is submitted that a fundamental difference between the present claimed invention and Koike is that the present invention uses a variable second threshold value in setting the horizontal image end signal (see e.g., page 41, lines 3 – 11), whereas in contrast Koike clearly indicates that the horizontal image start/end signals are determined based on the RGB data being larger than (for the start signal) or smaller than (for the end signal) a single predetermined threshold value (paragraphs 0038 and 0039).

The Examiner relies on col. 6, line 48, col. 7, line 42 of Koike in page 8 of the Action and basically asserts that since the frequency of the sampling clock is adjustable or variable based on the difference between the horizontal image start and end count values, then the threshold value for determining the horizontal image end signal is also adjustable.

However, it is respectfully submitted that the Examiner's position lacks any type of merit, since the predetermined threshold value for determining the horizontal image end signal is the same even if the frequency of the sampling clock is adjusted. That is, there is absolutely no change in the value used for determining the horizontal image end signal when the frequency of the sampling clock is adjusted, since this value remains constant at the predetermined threshold value, as explicitly disclosed in paragraph [0038] of Koike.

In contrast, in independent claims 1 and 3, the threshold value used for detecting the horizontal video end position of-the input video signal (the second threshold value) is controlled for each vertical period, depending on the level of the video data at the horizontal video end position detected within the verified period.

Specifically, in independent claims 1 and 3, the threshold value for detecting the horizontal video end position of the input video signal (the second threshold value) is variable, while in Koike it is fixed.

In claims 1 and 3, the second threshold value is controlled in that way. Therefore, as described on page 40, line 22 to page 41, line 11 of the specification, and as shown in Fig. 4, the second threshold value need not be set in conformity with a case where the input video signal is a signal having a low luminance, and can be set a large value. As a result, horizontal video effective periods L1 and L2 which are actually detected (see Fig. 4) are values closer to the

theoretical value L in the horizontal video effective period than that in the conventional example (Koike) (see Fig. 5).

Moreover, the Examiner's assertion in lines 13-16 of page 4 of the Action that the disclosure in col. 9, lines 51-col. 10, line 21 of Koike reads on the claimed threshold value control means also lacks any merit, since, as discussed above, the predetermined threshold value for determining the horizontal image end signal is the same even if the frequency of the sampling clock is adjusted. In other words, there is absolutely no need to include a threshold value control means in the device of Koike, since the threshold values are predetermined and do not change.

Accordingly, it is respectfully submitted that Koike fails to disclose or fairly suggest the features of the present claimed invention concerning a *horizontal video end position detection means for detecting a horizontal video end position of the video data outputted from the analog-to-digital converter on the basis of a variable second threshold value; ... threshold value control means for controlling, for each vertical period, the variable second threshold value depending on the level of the video data at the horizontal video end position detected within the vertical period.*

Accordingly, it is submitted that the features of the present claimed noted above would not have been obvious to one of ordinary skill in the art based on the teachings of Koike, and therefore the Examiner has failed to establish a prima facie case of obviousness.

Claims 5 and 6:

Independent claim 5 calls for *judgment means for judging for each field whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation means; and means for stopping, while the width of the region where the input video exists is being judged to be smaller than the number of horizontal effective pixels, a frequency adjustment operation based on the number of sampling clocks found in the field.* Independent claim 6 includes similar features.

In response to Applicants' argument that Koike fails to even addresses a situation involving a narrow video, since the behavior of the delay data generation unit stopping the delay control and issuing an instruction to terminate detection of the total of dots to the up-down counter (in Koike) has nothing to do with stopping frequency adjustment for narrow videos, the Examiner sets forth the following arguments on page 9 of the Action:

> As for the claimed judgement means Koike clearly teaches a comparator for determining for each field if the width of the region where input video exists is smaller than the number of horizontal effective pixels (1024, 1025) on the basis of the result of the calculation by the subtraction (153) as explained above. Where it is understood that the width of a region where input video exists corresponds to a display period, which would exist between the horizontal start and end position, which is taught by Koike.
>
> Further with reference to the means for stopping, Koike also clear teaches that the when the total of delay values becomes a predetermined value which is not less than a value corresponding to the one sampling clock, the delay data generation unit (62) stops delay control, and sends an instruction to terminate detection of the total of dots to the up-down counter (see column 10, lines 22-32). Therefore Koike teaches the claimed judgment means and means for stopping as explained above.

However, it is respectfully submitted that the judgement of the comparator 154 concerning whether the results of the subtraction sent from the subtractor 153 coincide with the number of horizontal effective dots, see paragraph [0075] of Koike, fails to constitute a determination of whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels, as called for in claim 5.

Moreover, even if, assuming *arguendo*, that the comparator 154 does provide a judgement regarding whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels, it is respectfully submitted that Koike clearly discloses that the comparator 154 brings a second judgement signal into an H level, paragraph [0077] when the results of the subtraction are smaller than "1024' and when the results of the subtraction in the subtractor 153 are smaller than "1024", the count value of the up-down counter 155 increases by one, so that the frequency division ratio of the frequency divider 14 also increases by one; such that as a result, the frequency of the sampling clocks outputted from the VCO 143 increases, see paragraph [0084].

In other words, when the number of sampling clocks is less than "1024", that is, assuming that this indicates that the width of a region where input video exists is smaller than the number of horizontal effective pixels, it is clearly disclosed in Koike that the frequency of the sampling clocks is increased and thereby adjusted, which is complete contrast to the present claimed invention.

Furthermore, it is respectfully submitted that the portion of Koike relied upon by the Examiner, i.e., col. 10, lines 22-32, concerns the situation when the first judgement signal is brought into an L level, when the results of the subtraction in the subtractor 53 coincide with "1024" or '1025," that is, when the width of a region where the input video exists is the same as the number of horizontal effective pixels.

The invention of claims 5 and 6 includes "the means for stopping, while the width of the region where the input video exists is being judged to be smaller than the number of horizontal effective pixels, a frequency adjustment operation based on the number of sampling clocks found in the field".

In contrast Koike does not have this means.

Since the invention of claims 5 and 6 comprises this "means for stopping ...", it is possible to suspend the frequency adjustment operation while video whose horizontal image start and end positions are difficult to detect, especially narrow video as generally seen on the screen saver image, is being inputted. This prevents erroneous operation.

Accordingly, it is respectfully submitted that Koike clearly fails to disclose or fairly suggest the features of the present claimed invention concerning *judgment means for judging for each field whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the*

calculation means; and means for stopping, while the width of the region where the input video exists is being judged to be smaller than the number of horizontal effective pixels, a frequency adjustment operation based on the number of sampling clocks found in the field.

Accordingly, it is submitted that the features of the present claimed noted above would not have been obvious to one of ordinary skill in the art based on the teachings of Koike, and therefore the Examiner has failed to establish a prima facie case of obviousness.

VIII. CONCLUSION

For the above reasons, Appellants request that the Board of Patent Appeals and Interferences reverse the Examiner's rejections of claims 1-6.

In the event this paper is not timely filed, appellants hereby petition for an appropriate extension of time. The fee for any such extension may be charged to our Deposit Account No. 50-2866, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

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Enclosures: Claims appendix
Evidence appendix
Related proceedings appendix

CLAIMS APPENDIX

Claim 1 (Previously Presented): A display device comprising:

a clock generation circuit for generating sampling clocks, whose frequency is controlled on the basis of a required frequency control value, on the basis of a horizontal synchronizing signal of an input video signal;

an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

horizontal video start position detection means for detecting a horizontal video start position of video data outputted from the analog-to-digital converter on the basis of a first threshold value;

horizontal video end position detection means for detecting a horizontal video end position of the video data outputted from the analog-to-digital converter on the basis of a variable second threshold value;

calculation means for calculating the number of sampling clocks corresponding to the distance from the horizontal video start position to the horizontal video end position;

judgment means for judging whether or not the result of the calculation by the calculation means coincides with a required reference value;

frequency control value adjustment means for calculating, when it is judged that the result of the calculation by the calculation means and the reference value do not coincide with each other, a new frequency control value on the basis of the result of the calculation by the calculation means, the reference value, and the frequency control value currently set in the clock generation circuit, to feed the new frequency control value to the clock generation circuit; and

threshold value control means for controlling, for each vertical period, the variable second threshold value depending on the level of the video data at the horizontal video end position detected within the vertical period.

Claim 2 (Original): The display device according to claim 1, wherein the clock generation circuit comprises

a voltage controlled oscillator for outputting the sampling clocks,

a frequency divider for dividing the frequency of the sampling clocks outputted from the voltage controlled oscillator,

phase detection means, to which an output of the frequency divider and the horizontal synchronizing signal of the input video signal are inputted, for outputting a detection signal corresponding to the phase difference between both the inputted signals, and

filter means for integrating the detection signal outputted from the phase detection means, to output the integrated detection signal to the voltage controlled oscillator, the frequency division ratio of the frequency divider being used as the frequency control value.

Claim 3 (Previously Presented): A display device comprising:

a clock generation circuit for generating sampling clocks, whose frequency is controlled on the basis of a required frequency control value, on the basis of a horizontal synchronizing signal of an input video signal;

an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

a horizontal video start position detection circuit for detecting a horizontal video start position of video data outputted from the analog-to-digital converter on the basis of a first threshold value;

a horizontal video end position detection circuit for detecting a horizontal video end position of the video data outputted from the analog-to-digital converter on the basis of a variable second threshold value;

a calculation circuit for calculating the number of sampling clocks corresponding to the distance from the horizontal video start position to the horizontal video end position;

a judgment circuit for judging whether or not the result of the calculation by the calculation means coincides with a required reference value;

a frequency control value adjustment circuit for calculating, when it is judged that the result of the calculation by the calculation circuit and the reference value do not coincide with each other, a new frequency control value on the basis of the result of the calculation by the calculation circuit, the reference value, and the frequency control value currently set in the clock generation circuit, to feed the new frequency control value to the clock generation circuit; and

a threshold value control means for controlling, for each vertical period, the variable second threshold value depending on the level of the video data at the horizontal video end position detected within the vertical period.

Claim 4 (Original): The display device according to claim 3, wherein the clock generation circuit comprises

a voltage controlled oscillator for outputting the sampling clocks,

a frequency divider for dividing the frequency of the sampling clocks outputted from the voltage controlled oscillator,

a phase detection circuit, to which an output of the frequency divider and the horizontal synchronizing signal of the input video signal are inputted, for outputting a detection signal corresponding to the phase difference between both the inputted signals, and

a filter circuit for integrating the detection signal outputted from the phase detection circuit, to output the integrated detection signal to the voltage controlled oscillator,

the frequency division ratio of the frequency divider being used as a frequency control value.

Claim 5 (Previously Presented): A pixel corresponding display device comprising

a clock generation circuit for generating sampling clocks on the basis of a horizontal synchronizing signal of an input video signal;

an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

detection means for comparing video data outputted from the analog-to-digital converter with a predetermined threshold value, to detect a horizontal video start position and a horizontal video end position on each of horizontal lines;

calculation means for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal out of horizontal video start positions detected within one field and a horizontal video end position farthest from the horizontal period start position specified by the horizontal synchronizing signal

out of horizontal video end positions detected within one field, the number of sampling clocks corresponding to the distance between the horizontal video start position and the horizontal video end position of the input video signal for the field;

frequency adjustment means for controlling the clock generation circuit on the basis of the result of the calculation by the calculation means, to adjust the frequency of the sampling clocks;

judgment means for judging for each field whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation means; and

means for stopping, while the width of the region where the input video exists is being judged to be smaller than the number of horizontal effective pixels, a frequency adjustment operation based on the number of sampling clocks found in the field.

Claim 6 (Previously Presented): A pixel corresponding display device comprising:

a clock generation circuit for generating sampling clocks on the basis of a horizontal synchronizing signal of an input video signal;

an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

a detection circuit for comparing video data outputted from the analog-to-digital converter with a predetermined threshold value, to detect a horizontal video start position and a horizontal video end position on each of horizontal lines;

a calculation circuit for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal out of horizontal video start positions detected within one field and a horizontal video end position farthest from a horizontal period start position specified by the horizontal synchronizing signal out of horizontal video end positions detected within one field, the number of sampling clocks corresponding to the distance between the horizontal video start position and the horizontal video end position of the input video signal for the field;

a frequency adjustment circuit for controlling the clock generation circuit on the basis of the result of the calculation by the calculation circuit, to adjust the frequency of the sampling clocks;

a judgment circuit for judging for each field whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation circuit; and

a circuit for stopping, while the width of the region where the input video exists is being judged to be smaller than the number of horizontal effective pixels, a frequency adjustment operation based on the number of sampling clocks found in the field.

Claim 7 (Original): A pixel corresponding display device comprising:

a delay circuit, whose amount of delay is variable, for delaying and outputting a horizontal synchronizing signal of an input video signal;

a clock generation circuit for generating sampling clocks which are synchronized with the horizontal synchronizing signal outputted from the delay circuit;

an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

detection means for comparing video data outputted from the analog-to-digital converter with a predetermined threshold value, to detect a horizontal video start position and a horizontal video end position on each of horizontal lines;

calculation means for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal outputted from the delay circuit out of horizontal video start positions detected within one field and a horizontal video end position farthest from a horizontal period start position specified by the horizontal synchronizing signal outputted from the delay circuit out of horizontal video end positions detected within one field, the number of sampling clocks corresponding to the distance between the horizontal video start position and the horizontal video end position of the input video signal for the field;

phase adjustment means for changing an amount of delay set in the delay circuit a predetermined amount at a time for each field, to change the phase of the sampling clocks a predetermined amount at a time for the field, holding as a first amount of delay the amount of delay set in the delay circuit in the field in a case where the number of sampling clocks calculated by the calculation means is changed in such a direction as to be decreased and holding as a second amount of delay the amount of delay set in the delay circuit in the field in a case where the number of sampling clocks calculated by the calculation means is changed in such a direction as to be increased, and calculating the average sum of the first amount of delay and the

second amount of delay, to set the amount of delay set in the delay circuit to the obtained average sum;

judgment means for judging for each field whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation means; and

means for stopping, when it is judged that the width of the region where the input video exists is smaller than the number of horizontal effective pixels, a phase adjustment operation based on the number of sampling clocks found in the field.

Claim 8 (Original): A pixel corresponding display device comprising:

a delay circuit, whose amount of delay is variable, for delaying and outputting a horizontal synchronizing signal of an input video signal;

a clock generation circuit for generating sampling clocks which are synchronized with the horizontal synchronizing signal outputted from the delay circuit;

an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit;

a detection circuit for comparing video data outputted from the analog-to-digital converter with a predetermined threshold value, to detect a horizontal video start position and a horizontal video end position on each of horizontal lines;

a calculation circuit for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal outputted from the delay circuit out of horizontal video start positions detected within one field

and a horizontal video end position farthest from a horizontal period start position specified by the horizontal synchronizing signal outputted from the delay circuit out of horizontal video end positions detected within one field, the number of sampling clocks corresponding to the distance between the horizontal video start position and the horizontal video end position of the input video signal for the field;

a phase adjustment circuit for changing an amount of delay set in the delay circuit a predetermined amount at a time for each field, to change the phase of the sampling clocks a predetermined amount at a time for the field, holding as a first amount of delay the amount of delay set in the delay circuit in the field in a case where the number of sampling clocks calculated by the calculation means is changed in such a direction as to be decreased and holding as a second amount of delay the amount of delay set in the delay circuit in the field in a case where the number of sampling clocks calculated by the calculation circuit is changed in such a direction as to be increased, and calculating the average sum of the first amount of delay and the second amount of delay, to set the amount of delay set in the delay circuit to the obtained average sum;

a judgment circuit for judging for each field whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation means; and

a circuit for stopping, when it is judged that the width of the region where the input video exists is smaller than the number of horizontal effective pixels, a phase adjustment operation based on the number of sampling clocks found in the field.

EVIDENCE APPENDIX

No evidence under 37 C.F.R. § 41.37(c)(1)(ix) is submitted.

RELATED PROCEEDING APPENDIX

No decisions under 37 C.F.R. § 41.37(c)(1)(x) are rendered.